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Procedia Engineering 30 (2012) 135 – 143

Procedia Engineering

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International Conference on Communication Technology and System Design 2011

Delay analysis of UDSM CMOS VLSI circuits

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Abstract

Propagation delay is one of the important issues for designing and synthesizing any VLSI circuits. In this paper, a simple and accurate delay model has been developed for Ultra Deep Sub-Micron (UDSM) CMOS inverter based on n^{th} power law of MOSFET model when the channel length is in the order of less than or equal to 90nm. Modified model is also applied in the CMOS NANAD2 and CMOS NOR2 in the UDSM range. All the parameters are extracted from BSIM.4.6.1 MOSFET user manual. This work derives analytical expression for the delay model of a CMOS inverter including all sorts of secondary effects such as Body Bias effect, Channel Length Modulation effect (CLM), Velocity Saturation effect, Drain Induced Barrier Lowering (DIBL), Gate Induced Drain Leakage (GIDL), etc which may be occurred in the UDSM MOS devices. Our result is better than nth power law and simulation results with respect to propagation delay time. Our proposed model gives an average error of 3.78% & 6.9% with compare to Cadence & Tanner Simulation results respectively.

Keywords: UDSM; BSIM; CMOS inverter; Sakuari Delay Model; Velocity Saturation effect.

1. INTRODUCTION

Delay analysis plays a very important role in the design and synthesis of CMOS VLSI circuits and systems. UDSM (Ultra Deep Sub-Micron) Technology deals with MOS devices with channel length in the order of 0.25µm to 0.022µm or even less [1-2]. As technology sizes continue to decrease (below 0.1µm or 100nm which is also known as Nano Technology), many new effects are being observed due to the use of UDSM technologies [3]. Power dissipation and delay are inversely proportional to each other for any CMOS devices. Integrated circuit designers have constantly required precise and proficient delay evaluation techniques that will help them to study a large variety of options and better utilization of the design space. Much of past research has addressed the issues of accurate and efficient delay modeling of VLSI circuits, but most of these methods are time and space consuming as well as include interpolation errors, i.e. none of these are cent percent applicable for Ultra Deep Submicron technology as all sorts of secondary effects

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doi:10.1016/j.proeng.2012.01.844

are not taken care off. This project will find a modified delay model for the UDSM-aware CMOS VLSI circuits like CMOS Inverter, NAND2, NOR2 etc considering all secondary effects (e.g. Body Bias effect, Channel Length Modulation effect (CLM), Velocity Saturation effect, Drain Induced Barrier Lowering (DIBL), Gate Induced Drain Leakage (GIDL) etc. We have taken the **nth power law** [4] of MOSFET model as the basis and include all the secondary effects that may be caused in nano-range to develop the more accurate model for the desired technology. All the expressions of different secondary effects are extracted from BSIM4.6.1 MOSFET models-user manual [5].

The paper is organized as follows. Section II presents different MOSFET models in literatures. In Section III, the modified nth power law Model has been proposed for CMOS inverter and also apply this to NAND and NOR CMOS circuits. Results are discussed in section IV. In section V, we analyzed the results with standard EDA tools Cadence & Tanner. Future work is discussed in section VI. Acknowledgement is given in VII.

2. Related work

As **Shockley Model** is very simple, many formulas have been derived based on the model, but the drain saturation voltage V_{DSAT} is different from the predicted value & the saturation region does not show Shockley's square-law dependence on gate–source voltage. So, this model is not satisfactory when applied to short channel MOSFET circuits [6]. Since Shockley's square law model is not accurate for UDSM MOSFETs due to velocity saturation, short channel effects, mobility degradation, etc are not included [3], a new MOSFET models have been developed which is known as **alpha-power law** [6]. This MOSFET model is the most widely utilized compact drain current model due to its simple mathematical form and high degree of accuracy. Moreover, the model does not describe the sub- threshold region and therefore on/off drain current tradeoffs cannot be thoroughly analyzed. MOS model takes into account the dependence of carrier mobility on the vertical field, carrier velocity saturation, and the dependence of the drain current on the transistor gate width (narrow-width effects) in [7-8]. Lots of research work on the delay model of CMOS Inverter has been proposed in [9-11].

The nth Power Law [4] MOS Model is developed by T. SAKUARI & A. R. Newton. The Drain current in three different regions (Cutoff region, Linear region & Saturation region) are given as follows:

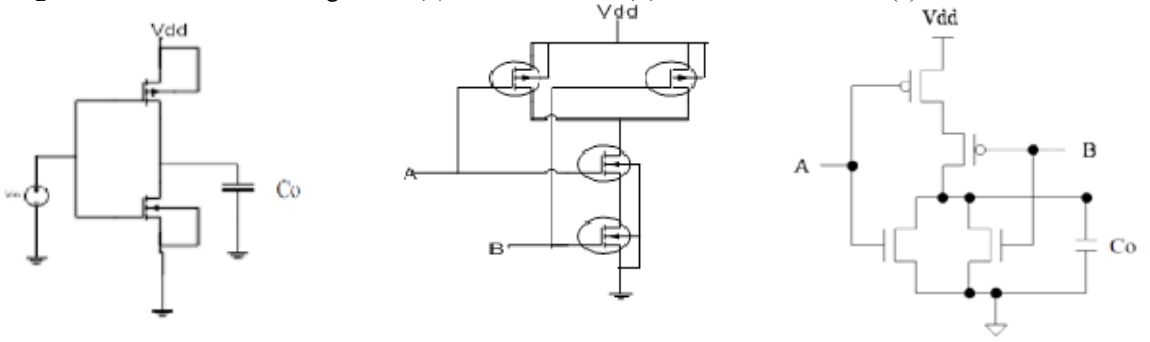
$$
\begin{aligned}
&V_{TH} = V_{TO} - \gamma 1 V_{BS} \\
&V_{DSAT} = K (V_{GS} - V_{TH})^{m} \\
&I_D = I_{DSAT} = \frac{W_{eff}}{L_{eff}} B (V_{GS} - V_{TH})^{n} \qquad \text{.....(1)} \\
&(V_{DS} \geq V_{DSAT} : Saturated\ region) \\
&I_D = I_{DSAT}\left(2 - \frac{V_{DS}}{V_{DSAT}}\right)\frac{V_{DS}}{V_{DSAT}} \quad (V_{DS} < V_{DSAT} : Linear\ region) \\
&I_D = 0 \quad (V_{GS} < V_{TH} : Cutoff\ region)
\end{aligned}
$$

Where, W_{eff} and L_{eff} are effective channel width and effective channel length, respectively. V_{T0} stands for zero back-gate bias threshold voltage and I_D is the drain current. Parameters K and m control the linear region characteristics while B and n determine the saturated region characteristics which describe the

short-channel effects in an empirical manner. The model reduces to the Shockley model for K = 1, m = 1, B = 0.5Kp, and n = 2 [12]. Others symbols notations are explained in Appendix. The propagation delay t_d, can be defined as time required to reach $0.5V_{DD}$ of output from the $0.5V_{DD}$ of input. **Sakuari Delay Model (developed from nth power law)** [12], is i. simple yet realistic, ii. Fast in evaluation, iii. Easy and fast to extract model parameters, & iv. Good for analytical treatment. This expression can not be used to model the inverter when the input rise-time is large or the fanout is small [13]. But this model is applicable for submicron the devices with channel length upto 0.5micron but not satisfied the delay of any Ultra Submicron CMOS devices.

3.Proposed delay model based on SAKAURI for CMOS inverter, CMOS NAND & CMOS NOR GATE

Fig1 shows the schematic diagram of (a) CMOS Inverter (b) CMOS NAND2 and (c) CMOS NOR2.



(a) (b) (c)

Fig1. Schematic diagram of a) CMOS Inverter b) NAND2 & c) NOR2

Based on **Sakuari Delay Model** [12]**,** we include the different secondary effects (Body Bias effect, CLM, Velocity Saturation effect, DIBL, GIDL, etc) that may occur in the nano-range. These effects are clearly explained in 'BSIM4.6.1 MOSFET Model' -User Manual [5]. In the following expressions, we introduced the different effects and extracted the parameters. From PTM technology we get all the parameters values. We compare our result with Sakurai and cadence with 90nm technology (UMC 90nm). The **Propagation delay of CMOS inverter** is given below (eq.1).

$$t_{PHL} = t_T \left\{ \frac{1}{2} - \frac{1-v_{T,n}}{n+1} + \frac{v_V - v_{T,n}}{n+1 \quad 1-v_{T,n}}^{n+1} \right\} + \frac{1}{2}\frac{C_0 V_{DD}}{I_{D0N}}$$

$$t_{PLH} = t_T \left\{ \frac{1}{2} - \frac{1-v_{T,p}}{n+1} + \frac{v_V - v_{T,p}}{n+1 \quad 1-v_{T,p}}^{n+1} \right\} + \frac{1}{2}\frac{C_0 V_{DD}}{I_{D0P}} \quad \text{.....(2)}$$

$$t_d = \frac{t_{PHL} + t_{PLH}}{2}$$

The expression for the input transition time (t_T) is given below:

$$t_T = \frac{C_O V_{DD}}{I_{DO}} \left(\frac{0.9}{0.8} + \frac{V_{DO}}{0.8 V_{DD}} \ln \frac{10 V_{DO}}{e V_{DD}} \right) \text{.....(3)}$$

The expression for critical transition time (t_{T0})

$$t_{T0} = \frac{C_O V_{DD}}{2 I_{DO}} \frac{(n+1)(-v_T)^n}{(-v_T)^{n+1} - (v_V - v_T)^{n+1}} \quad \text{.....(4)}$$

$$I_D = I_{DSAT} = I_{D0N/P} = \frac{W_{eff}}{2 * L_{eff}} (\mu_{eff} C_{ox}) (V_{GS} - V_{T,n/p})^{n_{N/P}} \quad \text{.....(5)}$$

The propagation delay for **2 inputs NAND (eq.6)** & **N-input NAND (eq.7)** gates are given below:

$$t_{PHL} = t_T \left\{ \frac{1}{2} - \frac{1-v_{T,n}}{n+1} + \frac{(v_{V,NAND} - v_{T,n})^{n+1}}{(n+1)(1-v_{T,n})^n} \right\} + \frac{1}{2} \frac{C_{total,nand2} V_{DD}}{I_{D0N}}$$

$$t_{PLH} = t_T \left\{ \frac{1}{2} - \frac{1-v_{T,p}}{n+1} + \frac{(v_{V,NAND} - v_{T,p})^{n+1}}{(n+1)(1-v_{T,p})^n} \right\} + \frac{1}{2} \frac{C_{total,nand2} V_{DD}}{I_{D0P}} \quad \text{.....(6)}$$

$$t_d = \frac{t_{PHL} + t_{PLH}}{2}$$

$$t_{PLH} = t_T \left\{ \frac{1}{2} - \frac{1-v_{T,n}}{n+1} + \frac{(v_{V,N-NAND} - v_{T,n})^{n+1}}{(n+1)(1-v_{T,n})^n} \right\} + \frac{1}{2} \frac{C_{total,nand-n} V_{DD}}{I_{DON}}$$

$$t_{PHL} = t_T \left\{ \frac{1}{2} - \frac{1-v_{T,p}}{n+1} + \frac{(v_{V,N-NAND} - v_{T,p})^{n+1}}{(n+1)(1-v_{T,p})^n} \right\} + \frac{1}{2} \frac{C_{total,nand-n} V_{DD}}{I_{DOP}} \quad \text{...(7)}$$

$$t_d = \frac{t_{PHL} + t_{PLH}}{2}$$

In similar way, Propagation delay equation for **2 inputs NOR (eq.8) & N-input NOR (eq.9)** gates are written below:

$$t_{PHL} = t_T \left\{ \frac{1}{2} - \frac{1-v_{T,n}}{n+1} + \frac{(v_{V,NOR} - v_{T,n})^{n+1}}{(n+1)(1-v_{T,n})^n} \right\} + \frac{1}{2} \frac{C_{total,nor2} V_{DD}}{I_{D0N}}$$

$$t_{PLH} = t_T \left\{ \frac{1}{2} - \frac{1-v_{T,p}}{n+1} + \frac{(v_{V,NOR} - v_{T,p})^{n+1}}{(n+1)(1-v_{T,p})^n} \right\} + \frac{1}{2} \frac{C_{total,nor2} V_{DD}}{I_{D0P}} \quad \text{....(8)}$$

$$t_d = \frac{t_{PHL} + t_{PLH}}{2}$$

$$t_{PLH} = t_T \left\{ \frac{1}{2} - \frac{1-v_{T,n}}{n+1} + \frac{(v_{V,N-NOR} - v_{T,n})^{n+1}}{(n+1)(1-v_{T,n})^n} \right\} + \frac{1}{2} \frac{C_{total,nor-n} V_{DD}}{I_{DON}}$$

$$t_{PHL} = t_T \left\{ \frac{1}{2} - \frac{1-v_{T,p}}{n+1} + \frac{(v_{V,N-NOR} - v_{T,p})^{n+1}}{(n+1)(1-v_{T,p})^n} \right\} + \frac{1}{2} \frac{C_{total,nor-n} V_{DD}}{I_{DOP}} \quad \text{....(9)}$$

$$t_d = \frac{t_{PHL} + t_{PLH}}{2}$$

3. Results & discussion

All the parameters are extracted from the 'BSIM4.6.1 MOSFET Model'- User Manual [5]. All values of model parameters are taken from Berkeley Predictive Technology Model (PTM) for 90nm technology (Beta Version, level 49) [14]. In all the cases we choose the value of W_p=5µm and W_n=2µm.

The fig2 shows that the propagation delay of CMOS Inverter, NAND2 & NOR2, how they are varying with respect to input transition time. By increasing the transition time the delay of UDSM circuits also increases. Due to series connection of two PMOS in NOR2 gate, the propagation delay time is higher than the NAND2 gate.

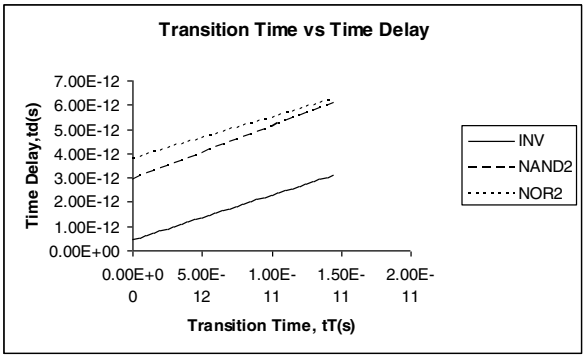


Fig2. Transition Time vs Delay Time of CMOS Inverter, NAND2 & NOR2

In fig3, how the delay time depends on inversion threshold voltage of CMOS Inverter, NAND2 & NOR2. Delay times enhanced by increasing the inversion threshold.

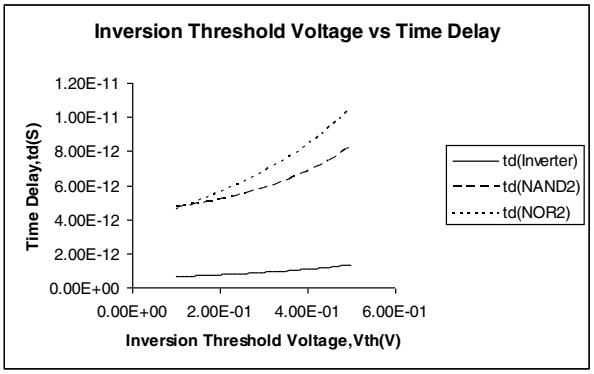


Fig3. Threshold Voltage vs Delay Time of Inverter, NAND2 & NOR2

Delay time also relate with Velocity saturation Coefficient of CMOS Inverter, NAND2 & NOR2 which is given in fig4. The delay increases due to increase of velocity saturation coefficient.

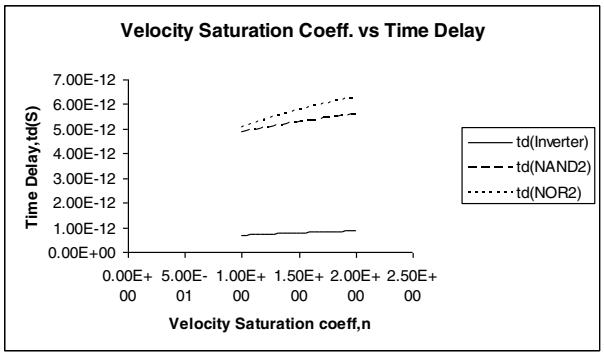


Fig4.Velocity Saturation Coefficient vs Delay Time of Inverter, NAND2 & NOR2

In fig5, delay time depends on width of MOS of CMOS Inverter, NAND2 & NOR2.

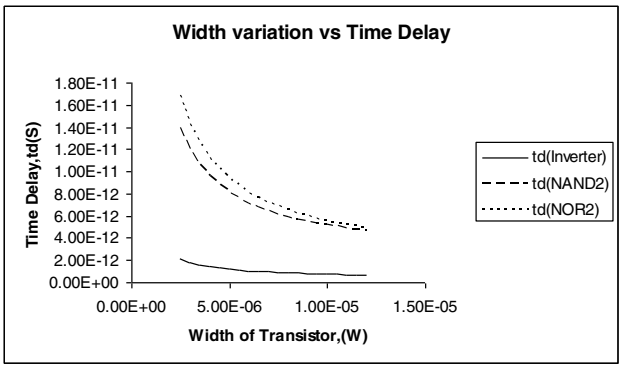


Fig.5. Transistor Width vs Delay Time of Inverter, NAND2 & NOR2

In fig6, delay time depends on load capacitance of MOS of CMOS Inverter, NAND2 & NOR2.

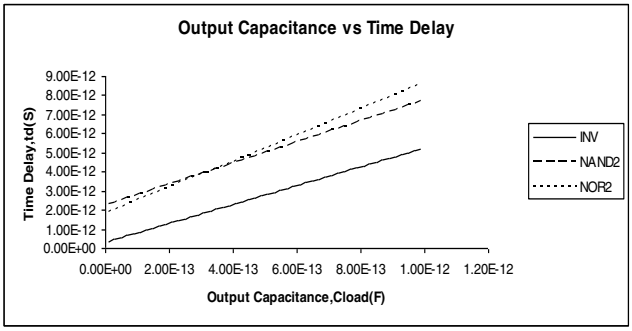
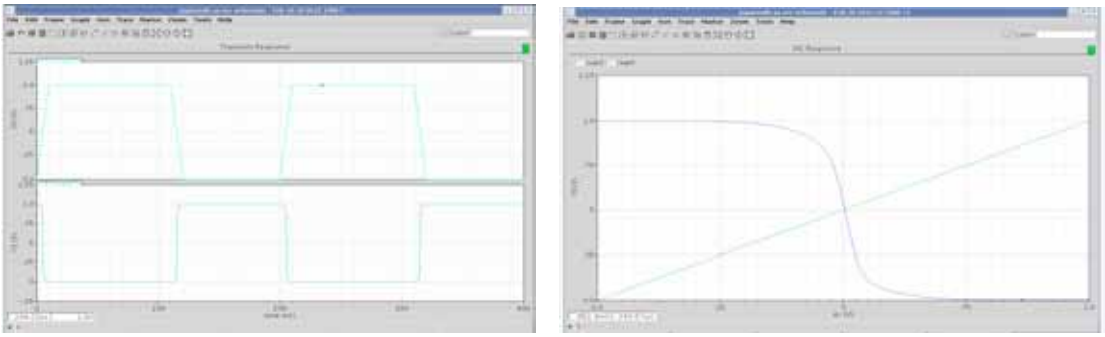


Fig.6. Load Capacitance vs Delay Time of Inverter, NAND2 & NOR2

In fig7, schematic snapshot of (a) Transient characteristic and (b) DC characteristic of CMOS inverter are taken from Cadence tool.



(a) (b)

Fig7. CMOS Inverter's (a) Transient characteristic & (b) DC characteristic

Fig8 shows the comparison graph among our proposed delay model, nth power law and simulation (Cadence & Tanner) result. It is clearly seen that the delay model results are nearly equal to cadence & Tanner simulation result. But the nth power law model result is far away from simulation results. The results differ due to the addition of different secondary effects which may occur in the UDSM range.

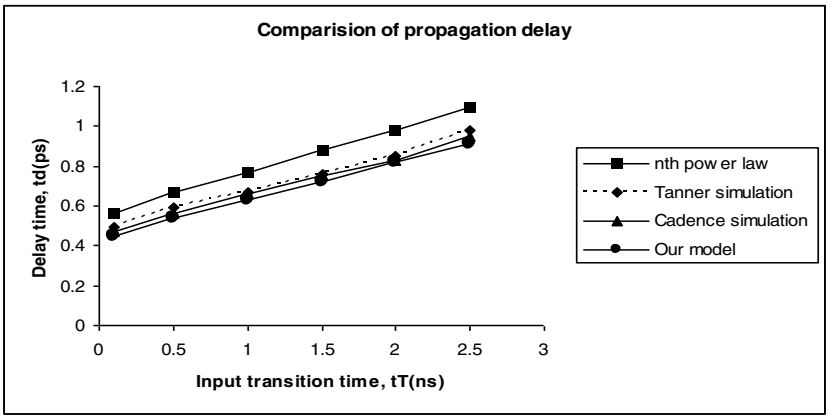


Fig8. Delay Comparisons for CMOS INVERTER (tT vs. td)

5. Result analysis

Table1-1. Delay Time and % of error for our proposed model, Simulation results (Cadence & Tanner) and nth power law:

Input Transition Time (ns)	% of error w.r.t. nth power law	% of error w.r.t. Tanner	% of error w.r.t. Cadence
0.1	24.44	8.89	4.44
0.5	24.07	9.26	3.70
1	22.22	6.35	4.76
1.5	22.22	5.56	4.17
2	19.51	3.66	1.22
2.5	19.78	7.69	4.40
Average Error	**22.04**	**6.90**	**3.78**

From the above table1-1, results are compared with nth power law and simulation results. It is noted that our model is close to result of Cadence simulation & Tanner simulation result with an average error of respectively 3.78% & 6.9%. On the other hand, average error for nth power law model is 22.04%. So it is seen that our model is more suitable in UDSM range than Sakurai delay model.

6. Future work

Applying this modified Delay model of the CMOS Inverter, 2-input NAND, and 2-input NOR, we will calculate the delay of any complex CMOS circuits like as XOR, XNOR, Half-Adder, Full-Adder etc. Finally, using this delay of above mentioned gates we can calculate the total delay of a sequential circuit like a Flip-flop, memory, Register etc. All the cases we will verify our result with Cadence simulation tool. We will further modify the delay model for greater accuracy.

7. Acknowledgments

Cadence simulation tool is accessed at IIT, KGP SMDP lab. Special thanks to Dr. D Samanta and Sk G Hossain for sharing their knowledge with me on this project. Thankful to my friend A Gupta for his help in programming part.

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9 appendix

In this paper, the used symbols are explained below:

t_{PLH} - Rising propagation delay: From input to rising output crossing $0.5V_{DD}$
t_{PHL} - Falling propagation delay: From input to falling output crossing $0.5V_{DD}$
t_d - average propagation delay: the delay from $0.5V_{DD}$ of input to $0.5V_{DD}$ of output
I_{D0N} -Saturated drain current of NMOS at $V_{GSN}=V_{DSN}=V_{DD}$
I_{D0P} -Saturated drain current of PMOS at $V_{GSN}=V_{DSN}=V_{DD}$
v_v -V_{INV}/V_{DD}, (V_{INV}=Logic Threshold Voltage of Inverter)

$v_{V,NAND}$ $-V_{NAND}/V_{DD}$(V_{NAND}=Logic Threshold Voltage of NAND2)
$v_{V,N\text{-}NAND}$ $-V_{N\text{-}NAND}/V_{DD}$($V_{N\text{-}NAND}$=Logic Threshold Voltage of N-input NAND)
$v_{V,NOR}$ $-V_{NOR}/V_{DD}$(V_{NOR}=Logic Threshold Voltage of NOR2)
$v_{V,N\text{-}NOR}$ $-V_{N\text{-}NOR}/V_{DD}$($V_{N\text{-}NOR}$=Logic Threshold Voltage of N-input NOR)
C_{ox} - Metal oxide capacitance
W_{eff} - Effective gate width
μ_{eff} - Effective mobility
V_{DO}-Drain saturation voltage when $V_{GS}=V_{DD}$
V_{DD} - Supply Voltage
V_{GS} – Gate to Source Voltage
C_O - Total Output Capacitance
$C_{total,nand2}$ & $C_{total,nand\text{-}n}$ – Total Output Capacitance of NAND2 gate & N-input NAND
$C_{total,nor2}$ & $C_{total,nor\text{-}n}$ – Total Output Capacitance of NOR2 gate & N-input NOR gate
$V_{T,p}$ & $V_{T,n}$- Threshold voltage of PMOS & NMOS
$v_{T,p}$ - $V_{T,p}/V_{DD}$
$v_{T,n}$ - $V_{T,n}/V_{DD}$
n - Velocity saturation coefficient, $(n_N+n_P)/2$
n_N - Velocity saturation coefficient of NMOS
n_P - Velocity saturation coefficient of PMOS
β - transconductance